**Micro Toddler ALU assignment**

This assignment is to create the ALU of the data path of Micro Toddler. The ALU consists of an integer adder along with a logic unit that can perform typical logic operation on the input arguments.

The diagram of the structure of the ALU is shown below



Using the logic unit adder and the previous mux\_2\_to\_1x16 implement this structure in a VHDL structural architecture and simulate it with the talu.vhdl testbench.

**INPUTS**

a,b : std\_logic\_vector (15 downto 0)

ltt : std\_logic\_vector (0 to 3)

Cin,arlo : std\_logic

**OUTPUTS**

res : std\_logic\_vector (15 downto 0)

Cout : std\_logic

Submit your code and simulation results in a .doc file to dropbox MTalu on CARMEN.